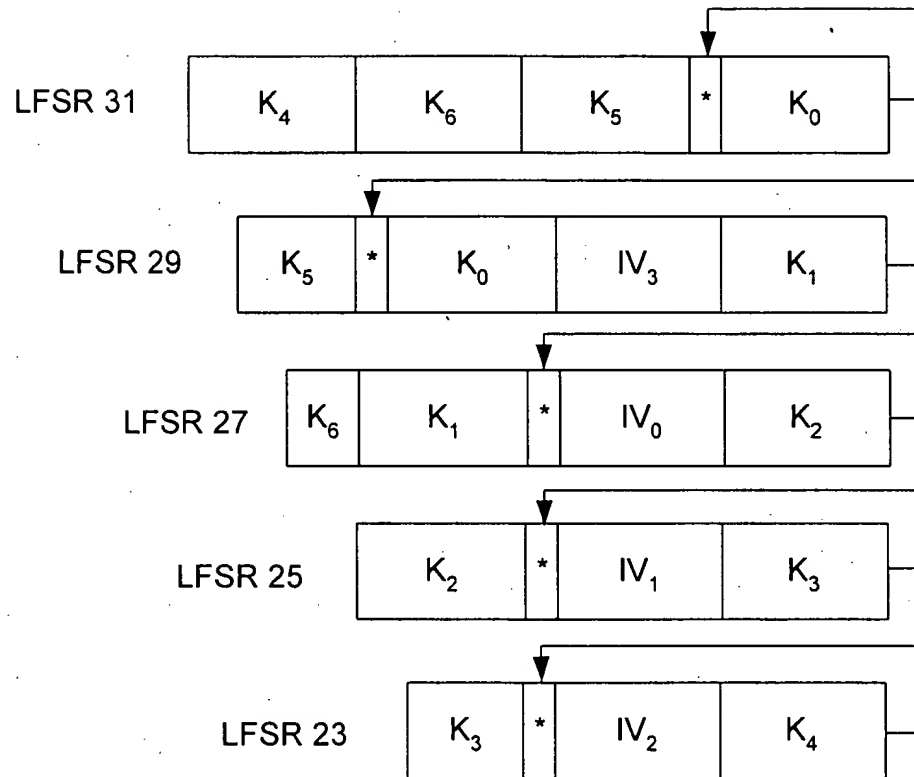


Fig. 1

## Initialization



\* Least significant bit of register is complemented

**Fig. 2**



09/452329

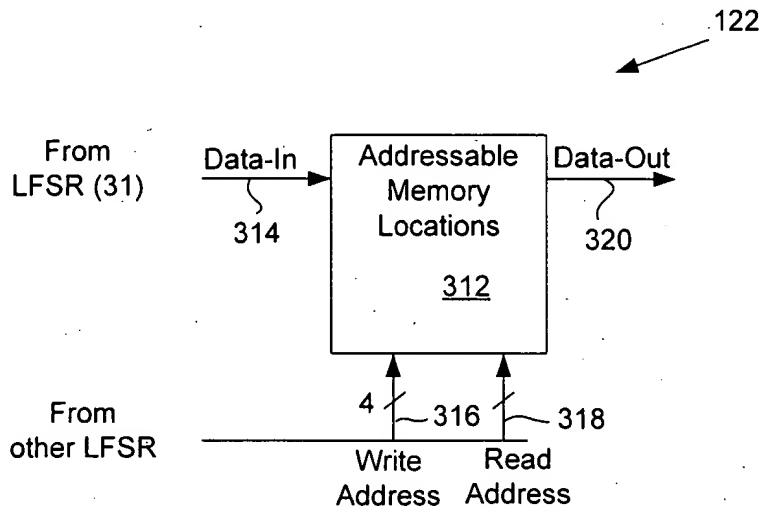


Fig. 3a

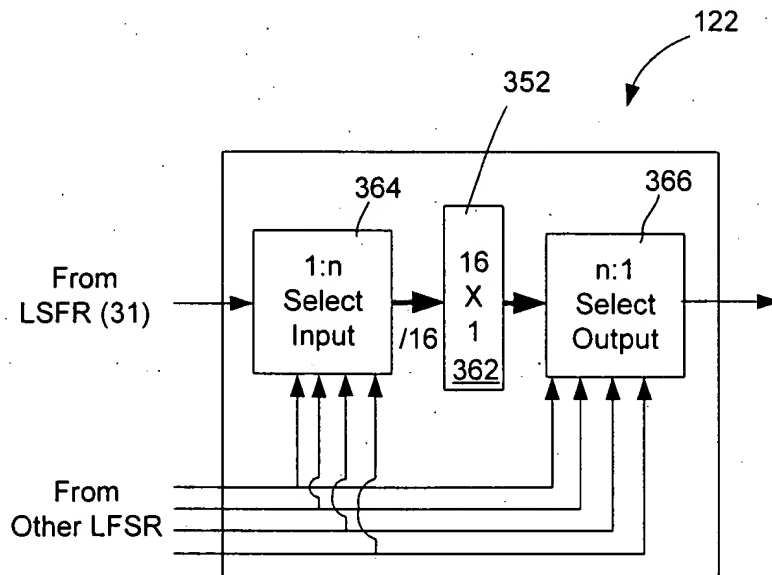


Fig. 3b